

## CLAIMS

We claim:

1        1.    An automatic gain control system comprising:  
2            an automatic gain control core circuit adapted to apply a  
3    gain to an input signal to provide an output signal;  
4            a power detector circuit adapted to receive the output  
5    signal and provide a first signal which indicates a power level  
6    of the output signal; and  
7            a processor adapted to control the gain of the automatic  
8    gain control core circuit based on the first signal.

1        2.    The system of Claim 1, further comprising an analog-  
2    to-digital converter adapted to receive the first signal from  
3    the power detector circuit and provide the first signal as a  
4    digital signal to the processor.

1        3.    The system of Claim 1, wherein the processor provides  
2    a calibration signal to the power detector circuit to calibrate  
3    a reference level for the system.

1        4.    The system of Claim 3, further comprising a digital-  
2    to-analog converter adapted to receive the calibration signal  
3    and provide the calibration signal as an analog signal to the  
4    power detector circuit.

1           5.     The system of Claim 3, further comprising:

2           a first switch, coupled between the processor and the power  
3     detector circuit, adapted to be closed by the processor during a  
4     calibration mode of the system to calibrate the reference level;  
5     and

6           a second switch, coupled between the automatic gain control  
7     circuit and the power detector circuit, adapted to be closed by  
8     the processor during a continuous automatic gain control mode of  
9     the system.

1           6.     The system of Claim 1, wherein the power detector  
2     circuit comprises:

3           a correlator; and

4           a low pass filter coupled to the correlator to determine  
5     the power level of the output signal.

1           7.     The system of Claim 1, wherein the processor provides  
2     a coarse gain control signal and a fine gain control signal to  
3     the automatic gain control core circuit to control the gain.

1           8.     The system of Claim 7, wherein the automatic gain  
2     control core circuit comprises a plurality of gain stages, with  
3     each of the gain stages having a plurality of transconductance  
4     stages.

1        9.     The system of Claim 8, wherein the fine gain control  
2 signal controls a bias current value for the transconductance  
3 stages, and the coarse gain control signal selects which of the  
4 transconductance stages contribute to the gain.

1        10.    The system of Claim 8, wherein the plurality of  
2 transconductance stages for each gain stage is associated with  
3 at least one load impedance.

1        11.    The system of Claim 10, wherein the load impedance  
2 comprises a shunt, a shunt-series, a series-shunt, a series-  
3 shunt-series, a T-coil, a T-coil with a cross-coupled capacitor,  
4 or a series-T-coil.

1        12.    An automatic gain control circuit comprising:

2        an amplifier adapted to apply a gain to an input signal to  
3 provide an output signal;

4        a detector adapted to receive the output signal and provide  
5 a first signal based on the output signal; and

6        a processor adapted to provide a coarse gain control signal  
7 and a fine gain control signal to the amplifier based on the  
8 first signal to control the gain of the amplifier, wherein the  
9 processor determines a reference level value for the output  
10 signal by providing a calibration signal to the detector and  
11 setting the reference level value based on the first signal.

1        13.    The circuit of Claim 12, wherein the detector is a  
2 power detector and the first signal is based on an average power  
3 level of the output signal.

1        14.    The circuit of Claim 12, wherein the detector is a  
2 peak detector and the first signal is based on a peak amplitude  
3 level of the output signal.

1        15.    The circuit of Claim 12, further comprising:

2        a digital-to-analog converter adapted to receive the  
3 calibration signal and provide the calibration signal as an  
4 analog signal to the detector; and

5        an analog-to-digital converter adapted to receive the first  
6 signal from the detector and provide the first signal as a  
7 digital signal to the processor.

1        16.    The circuit of Claim 12, wherein the detector is a  
2 power detector comprising a low pass filter coupled to a  
3 correlator.

1        17.    The circuit of Claim 12, wherein the fine gain control  
2 signal is set to minimize an absolute value of the first signal  
3 minus a reference value.

1        18. The circuit of Claim 12, wherein the amplifier  
2 comprises a gain stage, with the gain stage having a plurality  
3 of transconductance stages, wherein the fine gain control signal  
4 controls a bias current value for the transconductance stages  
5 and the coarse gain control signal controls which of the  
6 transconductance stages contribute to the gain of the amplifier.

1        19. The circuit of Claim 18, wherein the plurality of  
2 transconductance stages are associated with at least one load  
3 impedance.

1        20. The circuit of Claim 19, wherein the load impedance  
2 comprises a shunt, a shunt-series, a series-shunt, a series-  
3 shunt-series, a T-coil, a T-coil with a cross-coupled capacitor,  
4 or a series-T-coil.

1        21. A method of providing automatic gain control, the  
2 method comprising:

3        providing a gain to an input signal to provide an output  
4 signal;

5        monitoring a power level of the output signal; and

6        providing a coarse gain control and a fine gain control to  
7 control the gain based on the monitoring to maintain the output  
8 signal within a desired signal level range.

1        22.    The method of Claim 21, wherein the monitoring  
2 estimates an average power level of the output signal.

1        23.    The method of Claim 21, further comprising calibrating  
2 the monitoring to obtain a reference level value, with the  
3 desired signal level range based on the reference level value.

1        24.    The method of Claim 21, wherein the gain is performed  
2 in stages, with the coarse gain control and the fine gain  
3 control controlling a gain of each of the stages.

1        25.    A method of calibrating and monitoring an automatic  
2 gain control circuit, the method comprising:

3        providing a calibration signal whose signal level is  
4 estimated to provide a reference value;

5        setting a range for an output signal based on the reference  
6 value;

7        providing a gain to an input signal to provide the output  
8 signal;

9        monitoring an output signal level of the output signal; and

10       adjusting a coarse gain of the gain to maintain the output  
11 signal within the range.

1        26.    The method of Claim 25, further comprising setting a  
2 fine gain of the gain to minimize an absolute value of the power  
3 level of the output signal minus the reference value.

1        27.    The method of Claim 25, wherein the monitoring  
2 estimates an average power level of the output signal.

1        28.    The method of Claim 25; wherein the monitoring  
2 estimates a peak amplitude signal level of the output signal.